CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450.

T.E. GALBRAITH — 11/4/2005

Signature T.E. GALBRAITH — Date

Typed/Printed Name of Person signing Certificate

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of
Suresh Golwalkar et al
Filed 07/24/2001
Serial Number 09/911,918

Date: November 4, 2005
Group Art Unit 2873
Examiner: Jack Dinh
From: Tempe Arizona 85282

For: APPARATUS FOR COUPLING A FIBER OPTIC CABLE TO AN OPTOELECTRONIC DEVICE, A SYSTEM INCLUDING THE APPARATUS, AND A METHOD OF FORMING THE SAME

Declaration Pursuant to CFR 1.132

I, Dr. Kannan Raj declare as follows:

1. I am currently employed as a Technical Fellow at Primarion, a fabless semiconductor design company, In this role I am the Product Line Manager for all of Primarion's I/O products. I am an elected Sr. Member of the Institution of Electrical and Electronics Engineers (IEEE). I also serve on the Board of the Arizona Nanotechnology Cluster. I currently hold over 35 issued US and International patents. Also, I have authored/co-authored over 40 journal and conference publications.

2. My educational background is as follows: I have a Ph.D degree (1994) from the School of Information Technology and Engineering from George Mason

University, Fairfax, VA. I have an MSEE (1990) from Virginia Tech, Blacksburg, VA. I have an ME degree in Electrical Communication Degree from Indian Institute of Science, Bangalore (1988) and also hold a BS with Distinction in Applied Sciences from Anna University, Chennai (1984).

3. I have over 17 years of progressive experience in the semiconductor industry. For over 11 years I have worked as an engineer specializing in Semiconductor and optoelectronic system integration which includes packaging of components and sub-assemblies. For the past five years, I have been at Primarion, working on silicon design, fabrication, test and assembly. Prior to this I was at Intel corporation for nearly four years working on a variety of semiconductor product lines including processor and peripheral semiconductor components. Prior to this, I was a Research Assistant Professor at George Mason University. In this capacity, I held the dual role as project coordinator for the consortium in optical and optoelectronic technologies in computing (CO-OP). My role in the CO-OP was to bring together system and device researchers and enable the integration and packaging of emerging optoelectronic devices.

4. I am familiar with encapsulation processes in general and in particular with the encapsulation process described in the above referenced patent application. The encapsulation process as is known in the art of the semiconductor industry is done with the injection of a liquid polymer which then hardens and forms a plastic mold around the lead frames of the electrical conductors.

5. I have also read Henson et al US Patent 5,325,455. It is my understanding that this patent has been cited as a reference in the above identified patent application. This patent does not describe encapsulation. Moreover, item 14 in Figures 1 and 3 is not an "encapsulant" as that term would be understood by one skilled in the art. Rather, item 14 is a frame as described for example at column 4 lines 46, 64 and 68. Frame 14 cannot be an encapsulant because it is not introduced in liquid form to surround the components.

I hereby declare that all statements made herein of my own knowledge are true and that statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: 11/04/05

Dr. Kannan Raj